REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-8 are now in the application. Claims 1, 4 and 7 have been amended. New independent claim 8 has been added.

In item 3 on page 2 of the above-identified Office Action, claims 1-7 have been rejected as being anticipated by Nakashima (US Pat. 5,351,213) under 35 U.S.C. § 102 (b).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 12, lines 11-22 and page 8, line 5 to page 9, line 3 of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a memory circuit, having:

a plurality of write amplifiers for writing to a plurality of memory cells, each one of the plurality of write amplifiers assigned to a group of a plurality of bit lines; and

an address decoding circuit for simultaneously activating a group of the plurality of write amplifiers, depending on a test mode signal, so that the group of plurality of write amplifiers writes a test datum to a group of the plurality of memory cells via respectively assigned ones of the plurality of bit lines, **by masking a part of an address of the bit lines which is responsible for selection of a y-segment of the memory cell array.** (emphasis added)

The recited masking in the claims results in that the more significant y address bits are fixedly set to valid, so that all of the write amplifiers of each segment are selected in the event of an activated test mode signal TM.

This claimed feature is not disclosed in Nakashima.

The Nakashima reference discloses a semiconductor memory device which has an integral test circuit for generating test data to be batch written into the device's memory cells. The memory device has associated therewith sense amplifiers through which read/write operations are implemented. The test circuit tests each memory block.

New independent claim 8 makes it clear that that the memory circuit according to the present invention has a plurality of

write amplifiers, which are usually called secondary sense amplifiers, wherein each of the write amplifier is coupled to a number of primary sense amplifiers via respective switching devices. Thus, the primary sense amplifiers and the secondary sense amplifiers 5 are therefore almost directly coupled with one another, such that there is no unnecessary capacity or inductivity in the connection between the secondary sense amplifier and the primary sense amplifier.

In contrast thereto, Nakashima shows the primary sense amplifier 1, which apparently is coupled to a secondary sense amplifier (not shown) by a number of transistors 13, 14, 15, 16, 17, 18, which influence the electrical characteristic of the connection between the primary and the secondary sense amplifiers requiring added capacity or space and having increased inductivity relative to the present claimed invention.

A further advantage of the present claimed invention is that an existing memory circuit design can be used to operate a memory circuit in a test mode wherein a number of memory cells are simultaneously written.

Nakashima does not show "an address decoding circuit for simultaneously activating a group of said plurality of write

amplifiers, depending on a test mode signal, so that said group of said plurality of write amplifiers writes a test datum to a group of said plurality of memory cells via respectively assigned ones of said plurality of bit lines, by masking a part of an address of the bit lines which is responsible for selection of a y-segment of the memory cell array" as recited in claim 1 or 7 of the instant application.

Nor does Nakashima show "simultaneously activating a group of said plurality of write amplifiers, depending on a test mode signal, so that the group of the plurality of write amplifiers writes a test datum to a group of the plurality of the memory cells via respectively assigned ones of the plurality of bit lines, by masking a part of an address of the bit lines which is responsible for selection of a y-segment of the memory cell array" as recited in claim 4 of the instant application.

Nakashima does not show "a plurality of write amplifiers for writing to said plurality of memory cells, each one of said plurality of write amplifiers assigned to a group of said plurality of bit lines and coupled to primary sense amplifiers by respective switching devices" as recited in claim 8 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1, 4, 7, or 8. Claim 1, 4, 7, and 8 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 4.

In view of the foregoing, reconsideration and allowance of claims 1-7 together with new independent claim 8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made.

Payment in the amount of $200.00 for the additional independent claim in excess of three is enclosed herewith.

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Amdt. dated 2/15/06
Reply to Office action of 11/15/05

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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FDP/bb

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